ASHLING
EMBEDDED TECHNOLOGY AND INNOVATION

Ashling Application Note APB177

Using the Ashling Opella-XD Debug Probe with ARC™ Development Tools and Cores

1.1 Contents

1.2 Introduction

Ashling's Opella-XD for ARC Debug Probe, shown below, is a powerful JTAG Debug Probe for embedded development with ARC International's ARC 600/700, Energy PRO EP20/EP30 and ARCtangent-A4/A5 configurable RISC cores, with a high-speed USB 2.0 connection to the host PC.

Figure 1. The Ashling *Opella-XD for ARC* Debug Probe

Developed in co-operation with ARC International plc, the Opella-XD Debug Probe integrates with ARC's MetaWare IDE and provides powerful run/stop control of embedded software, with hardware and software breakpoints. Opella-XD is also supplied with the Ashling GDB Server which allows you to connect to your embedded target and debug using the GNU GDB debugger. Opella-XD provides fast code download to the target ARC system, and allows control and interrogation of all core-processor and system resources. In addition, Opella-XD supports FPGA Programming on the ARCangel Prototyping System or user's target board. Opella-XD works on both Windows and Linux hosted platforms.

This application note outlines the advantages of Opella-XD, shows how to use it with the MetaWare debugger and what debug connectors are needed on your target hardware.

1.3 Advantages of Opella-XD

This section summarises the advantages of using the Opella-XD Debug Probe, relative to simpler "parallel-port dongle" solutions.

1.3.1 USB connection to host PC

Opella-XD connects to the host PC using a compact and convenient USB link. Installation of parallel-port dongles, on the other hand, is subject to problems due to the number of different PC parallel-port implementations in use. In particular, reliability of parallel-port device drivers is problematical with Windows-NT, Windows-2000 or Windows-XP hosts. It can be very difficult to pinpoint the source of parallel-driver problems.

1.3.2 High-speed code communication to target

Opella-XD incorporates a high-speed, USB2.0 link for high-speed communication to the target, for both code download and FPGA "blasting". Using a 24MHz JTAG clock, Opella-XD downloads to the target at approximately 1275KB/s and reads-back data from the target at approximately 1293KB/s. Parallel-port cables are obviously limited by the speed of the software-driven parallel port. A parallel connection to ARCangel prototyping system communicates at less than 12KBytes/s; performance is even slower under Windows-98/NT/2000/XP due to the parallel-port driver.

1.3.3 Full control of JTAG communication clock

Opella-XD offers a choice of JTAG clock speeds for debug-communications to the target ARC processor. In contrast, parallel-port dongles provide no control over the JTAG clock; the clock must be generated by software on the PC. Thus, the user has no opportunity to "tune" the JTAG clock to optimize code download speed, or to operate with a target that uses a low frequency ARC processor clock.

Opella-XD supports JTAG clocks from 1kHz to 100MHz in finely grained increments. The very low JTAG speeds allow Opella-XD to work with hardware based simulation platforms whilst the high-speeds ensure optimum performance when working with actual silicon based designs.

Opella-XD supports use of a Returned TCK signal (RTCK). When enabled, Opella-XD will wait for RTCK before sending a subsequent TCK pulse. This feature supports targets that go into sleep or power-down modes.

1.3.4 Full Multi-Core Debug support

Opella-XD offers full support multi-core target systems (where the ARC processors are on the same JTAG chain). In addition, multiple Opella's can be connected to a single PC for multi-core target systems with a unique JTAG chain for each ARC processor.

1.3.5 Readymade Debug Probes

Opella-XD is supplied with TPAOP-ARC20, a 20-pin .1" JTAG probe cable that allows direct connection to the ARC processor (in a custom FPGA or in final silicon) on the user's target board. A D15 adapter, AD-ARC-D15, can be used with TPAOP-ARC20 to connect to the D15 JTAG socket on ARC International's ARCangel prototyping system. Parallel-port dongles, on the other hand, are supplied with flying leads only; the user is left with the task of building the debug connector. See
ARC Processor Debug Connections for full details on target interfacing.

1.4 Benefits of Opella-XD as a debug platform

Taken together, the performance advantages of Opella-XD mean that it is the recommended vehicle for real-time debugging on ARC systems, with benefits that include:

1. Plug-and-play installation, with a convenient Setup program and USB auto-detect, ensures that installation time is minimized.
2. High-speed download minimizes time lost when download large code images or FPGA configurations.
3. Choice of JTAG clock speeds (from 100MHz down to 1kHz) ensures reliable performance with high-speed and low-speed target systems.
4. No problems with low-voltage targets: Opella's 20-pin target probe cable automatically adapts to target logic levels in the range 0.9V to 3.6V.
5. Powerful Diagnostic utilities to confirm target JTAG communications, ARC processor (register) access and target memory access.
6. Fully engineered Target Probes, with complete interface documentation, provide plug and-play operation when debugging on ARCangel prototyping system, on a custom FPGA implementation and on final custom silicon.
7. Integrated into MetaWare and GNU GDB Debuggers.
8. Access to Ashling's ARC Engineering team for support.

1.5 Ashling Opella-XD for ARC Diagnostic Utility

The Ashling Opella-XD for ARC Diagnostic Utility (`OPXDARC.EXE`) allows you to confirm proper installation and operation of Opella-XD for ARC by selecting the **Ashling Opella-XD for ARC Diagnostic Utility** shortcut from the **Ashling Opella-XD for ARC** group on your programs start menu.

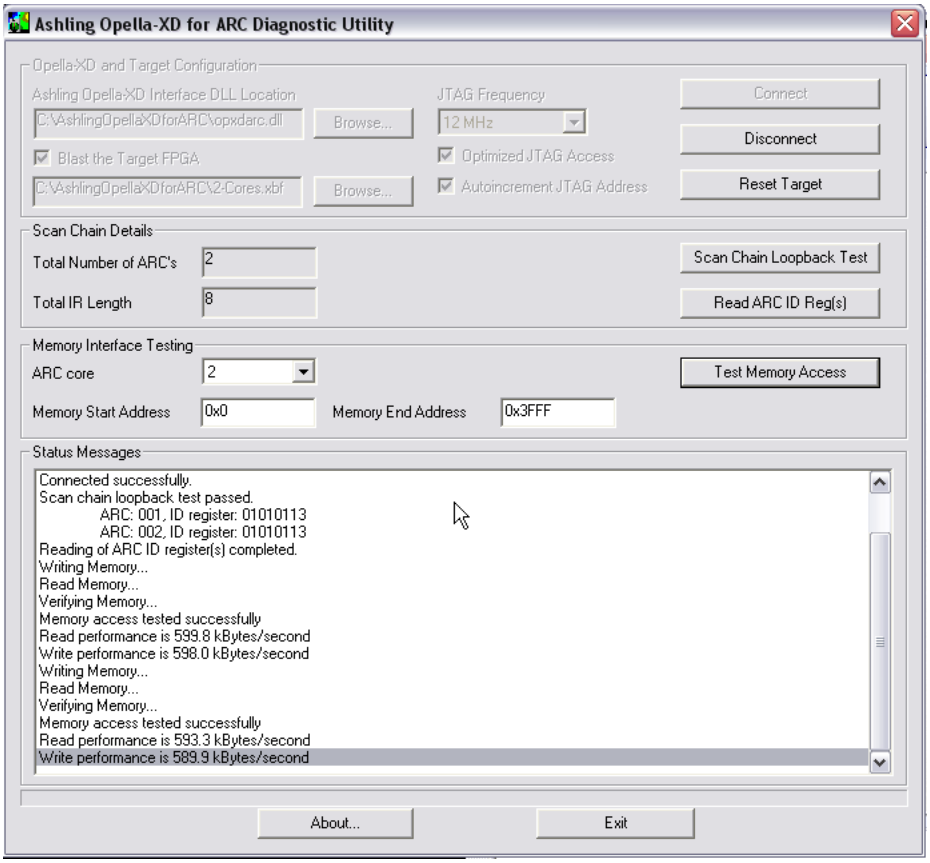

Figure 2. Ashling Opella-XD for ARC Diagnostic Utility

The utility allows you:

1. Blast (program) your target FPGA
2. Perform scan chain testing to verify basic JTAG communication between Opella-XD and your target and that your target JTAG scan-chain is functional
3. Read and display the Auxiliary Identity register of each ARC processor on the scan-chain.
4. Test memory interfacing for a defined address range and benchmark memory read/write performance

1.6 ARC MetaWare Debugger (mdb.exe) Configuration

Opella-XD works with ARC's MetaWare Debugger (`mdb.exe`) and can be easily configured as shown in the following steps (screen-shots shown based on MetaWare Debugger v8.1.2):

1. Run the MetaWare Debugger and the **Debug a process or processes** dialog is show as follows:

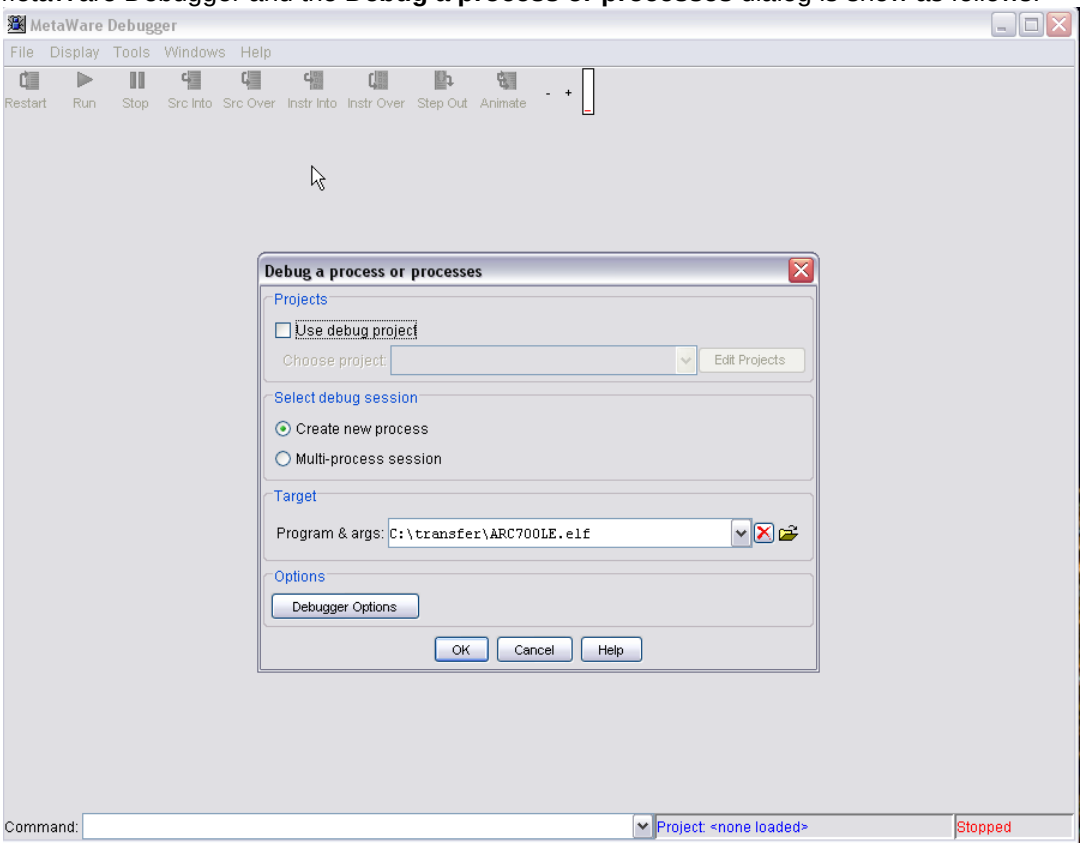

Figure 3. Debug a process or processes dialog

Select the program you want to debug using **Program & args** and click the **Debugger Options** button which brings up the dialog as follows.

Select **Target Selection** in the left-hand column to configure your Opella-XD as shown below:

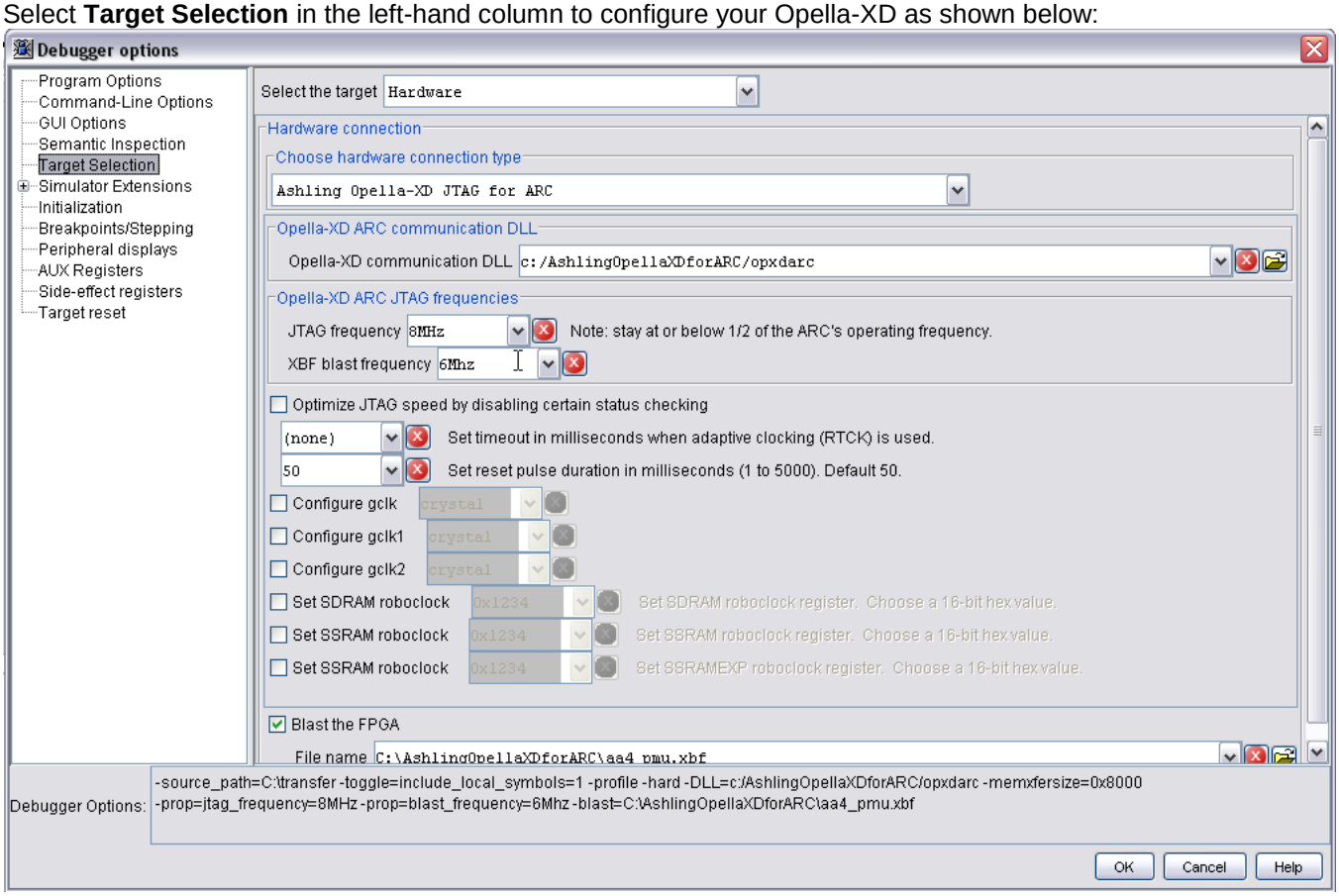

Figure 4. Debugger options|Target selection dialog

Select **Ashling Opella-XD JTAG for ARC** as the hardware connection type. Set **Opella-XD ARC communication DLL** to the location of your Opella-XD MetaWare Debugger Driver DLL (by default, `OPXDARC.DLL` which is stored in `\AshlingOpellaXDforARC`).

2. Opella's JTAG frequency can be specified via **JTAG frequency**. It's best to set up your system initially with a low JTAG clock frequency, such as 1 MHz. Once you have established communication with the target, you can increase the JTAG clock to the highest frequency that maintains stable, consistent operation of the emulator and debugger. You should not select a JTAG frequency that is more than half of the ARC processor's clock frequency.

3. If you want Opella-XD to program your target FPGA, then check **Blast the FPGA** and specify the blast file name.

4. Click on **OK** when finished. This returns you to the **Debug a process or processes** dialog:

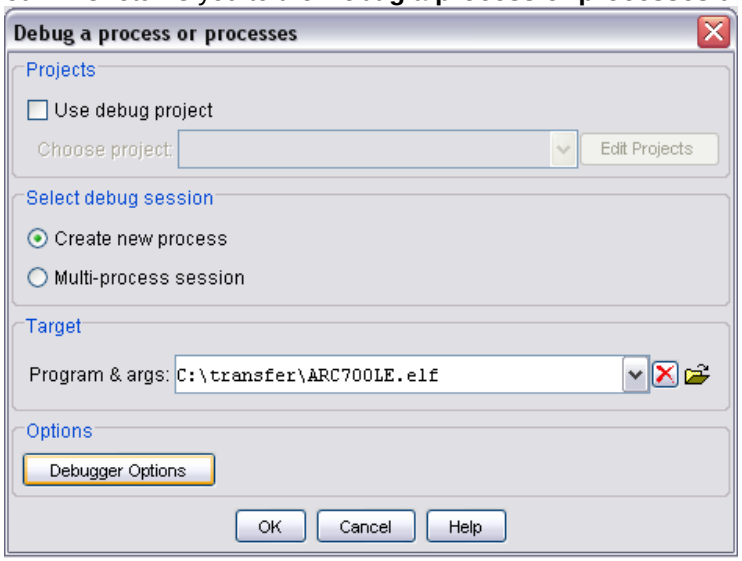

Figure 5. Debug a process or processes dialog

Click **OK** and you will then be presented with the **Ashling Opella-XD Configuration** dialog as follows:

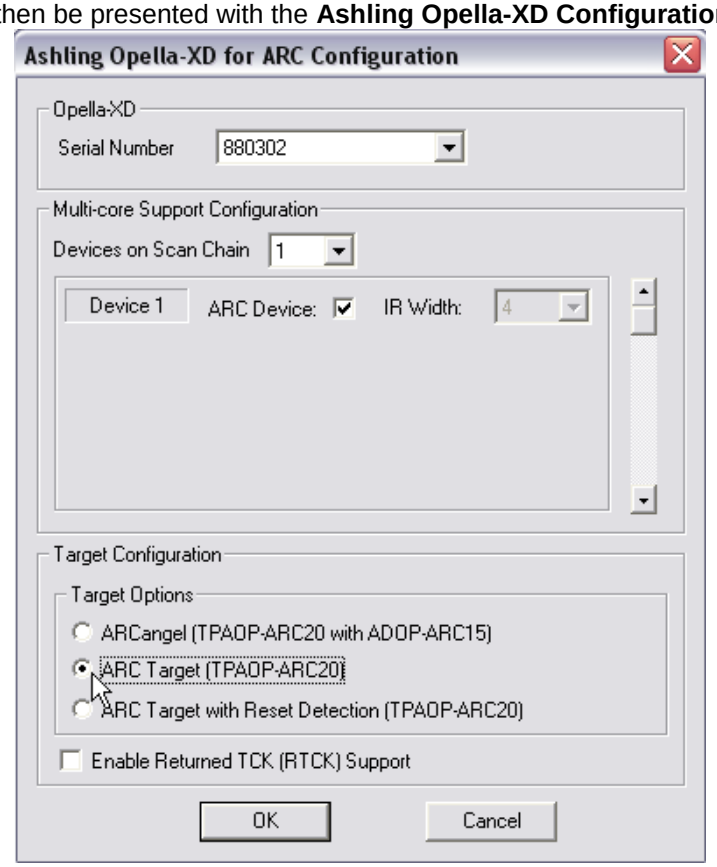

Figure 6. Ashling Opella-XD Configuration dialog

This dialog allows you to:

- Specify the Opella-XD you wish to connect to via the **Opella-XD** group. If you have multiple Opella's connected to your PC then this group allow you to specify which Opella-XD to use. Opella's are numbered by their serial number.
- If your target system has multiple devices on the JTAG scan-chain then you need to specify the configuration of your scan-chain using the **Multi-Core Support Configuration** group**.** Specify the number of **Devices on Scan Chain** and type of each device (i.e. **ARC** core or not); for devices that are not ARC cores you will need to specify the JTAG Instruction Register **IR Width** (typically, this is 4 bits).
- The **Target Configuration** options allow to configure the following options:
    - **ARCangel** should be selected when connecting to the ARCangel Prototyping System via a TPAOP-ARC20/AD-ARC-D15 Target Probe Assembly (Opella-XD cable).
    - **ARC Target** should be selected when connecting to an ARC target via the TPAOP-ARC20 TPA.
    - **ARC Target with Reset Detection** should be selected when connecting to an ARC target via the TPAOP-ARC20 TPA. This option ensures that Opella-XD will automatically detect a target reset on pin 15 (RST*).
    - **Enable Returned TCK (RTCK) Support** allows support for target systems that provide a returned TCK (RTCK) via pin 11**.** When selected, Opella-XD will wait for RTCK before sending a subsequent TCK pulse. RTCK is only supported when using the TPAOP-ARC20 Opella cable.

Please Note*: If you wish to prevent this dialog popping up then edit OPXDARC.INI and set* `ShowConfiguration` *to 0 as follows:*

```
[MiscOptions]
ShowConfiguration=0
```

This will prevent the dialog popping up (default or last settings will be used).

Click **OK** when you are complete. Your are now ready to being debugging using the MetaWare Debugger and the Ashling Opella-XD Debug Probe.

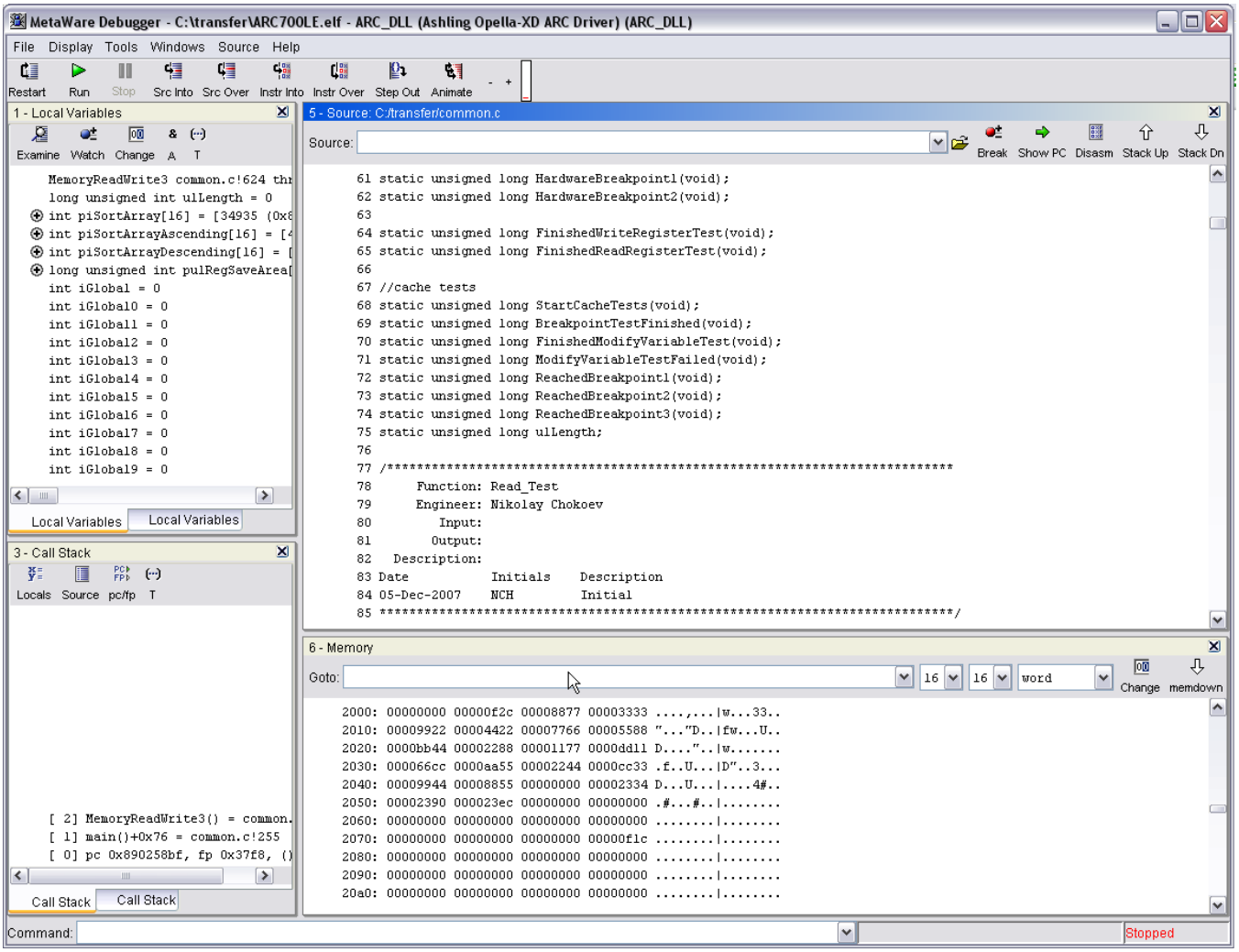

Figure 7. MetaWare Debugger

1.7 Using Opella-XD with the GNU GDB Debugger

The Ashling GDB Server allows you to use Opella-XD to connect to your embedded target and debug using the GNU GDB debugger.

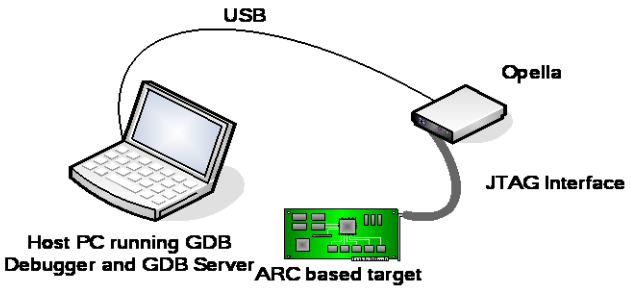

Figure 8. Using the Ashling GDB Server

The Ashling GDB Server is a console type application hosted on either Windows™ or GNU/Linux x86 based PCs. It takes requests from the GDB Debugger and sends them directly to the Opella-XD Debug Probe. In the above figure, the GDB Debugger and Server are shown running on the same PC, however, this is not a requirement and the GDB Server can reside on any machine that has a network connection to the machine running the GDB Debugger (as the Server communicates to the Debugger using the TCP/IP protocol). The Ashling GDB Server supports any debugger that adheres to the GDB Remote Serial Protocol including:

- GDB version 5 or later
- Eclipse CDT

In addition, the GDB server supports multi-core debugging is supporting by running multiple instances of the debugger. For more information and some examples on using the GDB server please refer to the supplied Ashling User Manual.

1.8 Obtaining latest Opella-XD software

The latest versions of software are available on the Ashling ARC Tools support Web site at:

www.ashling.com/support/ARC/index.html

You must have an existing Software Upgrade Service ("SUS") contract from Ashling to allow access to this site. Contact your local Ashling representative for details (see www.ashling.com for Ashling contact details).

1.9 ARC Processor Debug Connections

For the hardware connection to your ARC target, Ashling offers a choice of Probe Cables:

1. **TPAOP-ARC20** 20-pin .1" JTAG probe cable, for connection to a 20-pin JTAG pin-strip on your custom target board; this cable can be used for debugging an ARC core in a custom FPGA or in final silicon. When used with Opella-XD, this cable automatically adapts to target logic levels in the range 0.9V to 3.6V.
2. **AD-ARC-D15** D15 adapter. This allows a TPAOP-ARC20 TPA to be connected to the D15 JTAG socket on the ARCangel Prototyping Unit.

1.9.1 ARC Debug Connections

ARC cores (and the ARCangel prototyping system) implement a debug module that uses the JTAG serial interface which is supported on Ashling's range of Debug Probes for the ARC architecture.

1.9.1.1 ARCangel Debug and FPGA blasting probe connections

This section describes the recommended connector for the Ashling D15 JTAG probe cable, for use with the ARCangel Prototyping platform (or with user boards that use the same connection scheme as ARCangel, using 3.3V logic levels on the debug interface).

Ashling's **AD-ARC-D15** Target Probe Assembly contains a D15 Male free plug (see Figure 9) that connects to the D15 Female fixed socket on ARCangel. Pin connections for this connector are shown in tabular form in Table 1.

Pin	Signal	Function (Debugging and FPGA blasting on ARCangel board)	Function (Debugging only)	Direction
1	FPGA_DATA (D0)	Downloaded FPGA data (ARCangel only)	Unused	Input (to Target from Debug Probe)
2	FPGA_CLK (D1)	FPGA programming clock (ARCangel only)	Unused	Input (to Target from Debug Probe)
3	Unused (D2)			
4	Unused (D3)			
5	Unused (D4)			
6	SS0	ARCangel configuration bit 0 (ARCangel only)	ARCangel configuration bit 0 (ARCangel only)	Input (to Target from Debug Probe)
7	SS1	ARCangel configuration bit 1 (ARCangel only)	ARCangel configuration bit 1. Pulling this pin low will reset the ARC target. (ARCangel only)	Input (to Target from Debug Probe)
8	CNT	ARCangel control (ARCangel only)	ARCangel control (ARCangel only)	Input (to Target from Debug Probe)
9	DONE	ARCangel FPGA programmed OK (ARCangel only)	Unused	Output (from Target to Debug Probe)
10	TDI	JTAG test data in	JTAG test data in	Input (to Target from Debug Probe)
11	TMS	JTAG test data mode in	JTAG test data mode in	Input (to Target from Debug Probe)
12	TDO	JTAG test data out	JTAG test data out	Output (from Target to Debug Probe)
13	GND	Ground	Ground	
14	TCK	JTAG clock	JTAG clock	Input (to Target from Debug Probe)
15	GND	Ground	Ground	

Table 1: Pin connections on Ashling's AD-ARC-D15 Probe Assembly for use with ARCangel

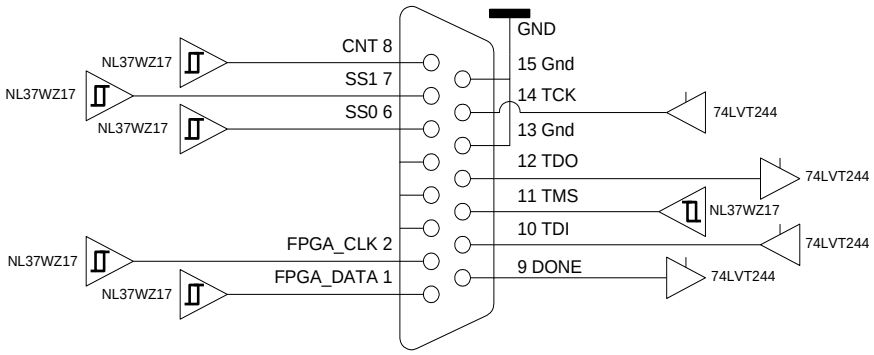

Figure 9. Pin-out of Ashling D15 JTAG Probe, for use with ARCangel

The drive capability of the AD-ARC-D15 Probe is shown in Table 2.

	Load	**Low-state**	**High-state**
Input pins 1, 2, 6, , 11 (to Device from Debug Probe): Debug Probe drive characteristics		-24mA drive @ 0.55V max; or -100µA drive @ 0.1V max.	+24mA drive @ 2.3V min; or +100µA drive @ 3.2V min.
Input pins 7, 8, (to Device from Debug Probe): Debug Probe drive characteristics		Open-drain	470k pull-up
Input pins 10, 14 (to Device from Debug Probe): Debug Probe drive characteristics		-32mA drive @ 0.5V max; or -100µA drive @ 0.2V max.	+32mA drive @ 2.0V min; or +100µA drive @ 3.1V min.
Output pins 9, 12 (to Debug Probe from Device): Debug Probe termination characteristics	±500 µA termination current while switching	0.8V max.	2.0V min.

Table 2: Ashling D15 JTAG Probe drive and termination characteristics

The on-chip driver and receiver pads, and the on-chip and off-chip pull-up or pull-down resistors, must be chosen so as to ensure adequate signal transitions to the Debug Probe (on Output pins) and to correctly sense logic voltages from the Debug Probe (on Input pins). The ARCangel Prototyping System meets these requirements.

1.9.1.2 Alternative direct debug connection to ARC target systems

For use on an SoC design that has been implemented as a self-contained FPGA, *or* for debugging on a "real" ARC-core silicon SoC, you can use *either* the D15 JTAG Probe connections in section 1.9.1.1, *or* you can use the simpler 20-pin .1" connection arrangement in this section. Note that this 20-pin connector does not support FPGA blasting. When used with Opella-XD, this cable automatically adapts to logic levels on the target debug interface in the range 0.9V to 3.6V. Ashling's **TPAOP-ARC20** Target Probe Assembly contains a 20-pin double-row .1" female free socket that can connect to a male 20-pin JTAG pin-strip on your custom target board:

Pin	Signal	Function	Direction
1	Vtref	Target reference voltage; used by the Debug Probe to sense target voltage and adjust probe voltages accordingly (see Note 1).	From target to Opella-XD
2	Reserved	***Do not connect to this pin***	-
3	Reserved	***Do not connect to this pin***	-
4	GND	Ground	-
5	TDI	JTAG test data in (see Note 2).	From Opella-XD to target
6	GND	Ground	-
7	TMS	JTAG test data mode in (see Note 1).	From Opella-XD to target
8	GND	Ground (see Note 4).	-
9	TCK	JTAG clock (see Note 1).	From Opella-XD to target
10	GND	Connect to ground on target	-
11	GND/RTCK	If you are using a device with an RTCK signal then connect it to this pin. Each time Opella-XD sends a TCK pulse it will wait for RTCK pulse before continuing. If you are not using a device with RTCK then connect this pin to ground on the target.	From target to Opella-XD
12	GND	Connect to ground on target	-
13	TDO	JTAG test data out	From target to Opella-XD
14	Reserved	***Do not connect to this pin***	-
15	RST*	This pin works in two different modes: • **ARC Target with Reset Detection**. When this mode is enabled this pin is an input and used to detect a ARC core reset. • **ARC Target**. When requested by the MetaWare Debugger, Opella-XD will activate this signal (pull down then release). (see Note 3).	Bi-directional From Opella-XD to target From Opella-XD to target
16	Reserved	***Do not connect to this pin*** held at logic-low by Opella-XD	-
17	Reserved	***Do not connect to this pin***	-
18	GND	Connect to ground on target	-
19	Reserved	***Do not connect to this pin***	-
20	GND	Connect to ground on target	-

Table 3: Pin connections on Ashling's TPAOP-ARC20 Probe Assembly for use with custom target ARC boards

Note 1: To provide a defined state on the debug-input pins to the ARC core when the Debug Probe isn't connected, pull-down resistors should be fitted on the TDI, TMS and TCK pins on the target board (typically 10KΩ).
Note 2: The Debug Probe applies load of 200KΩ or greater (25µA or less) to Pin 1. This line should be connected to Vcc on the target board (a buffer resistor of not more than 100Ω can be used in series, but is not required).
Note 3: This signal is an open-drain output with an internal 470KΩ pull-up to an internal voltage equivalent to Vtref. In addition, there is a 3.3Ω series resistor. The Target must provide a pullup to Vcc (minimum 4.7KΩ, maximum 1mA) on this pin.
Note 4: The Opella-XD holds these pins at logic-low potential. Connect these pins to Ground on the target board.

The following figure shows the pin-out of the 20-way TPAOP-ARC20:

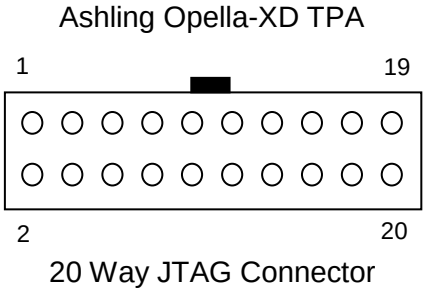

Figure 10. Pin-out of Ashling's TPAOP-ARC20 Probe Assembly for use with custom target ARC boards

Your target board should have a JTAG connector as follows:

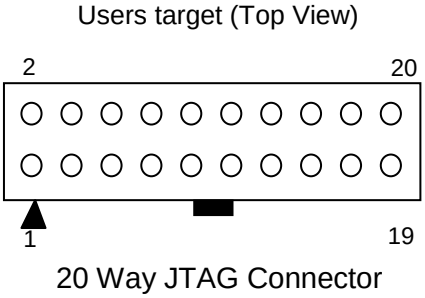

Figure 11. Pin-out of 20-way JTAG connector on your target ARC board

The drive capability of the Opella-XD-ARC Debug Probe when connected to the **TPAOP-ARC20** Target Probe Assembly is shown in Table 4.

	Load	Low-state	High-state
VTref Output pin (to Debug Probe from Target): Debug Probe termination characteristics	200KΩ to ground		
TDI, TMS and TCK Input pins (to Target from Debug Probe): Debug Probe drive characteristics		-24mA drive @ 0.55V max; or -100µA drive @ 0.2V max.	+24mA drive @ 2.0V min; or +100µA drive @ Vcc – 0.2V min.
TDO Output pin (to Debug Probe from Target): Debug Probe termination characteristics	±5 µA termination current	0.7V max.	1.7V min at Vcc 2.3V; 2.0V min at Vcc 2.7V
RST* Input pin (to Target from Debug Probe): Debug Probe drive characteristics		105Ω @ –2mA max.	1.1KΩ to +3.3V

Table 4: Ashling Opella-XD ARC Debug Probe drive and termination characteristics, when connected to TPAOP-ARC20 Target Probe Assembly

1.9.2 Target voltage interfacing

The Ashling tools for ARC-architecture debugging support 0.9V to 3.6V target systems, when connected to the target using the TPAOP-ARC20 20-pin .1" Target Probe Assembly. The tools automatically adjust their logic interface levels to cater for the target's levels. The **AD-ARC-D15** Target Probe Assembly supports ARCangel (or ARC) targets at 3.3V.