

Opella-XD for RISC-V



High-performance Ashling JTAG debug probe

Overview

Opella-XD is Ashling's high-performance JTAG debug probe for embedded development on devices based on the RISC-V open Instruction Set Architecture.

The Opella-XD hardware debug probe is part of a range of tools provided by Ashling for development on RISC-V including IDE, compiler, simulator and debugger. It integrates with Ashling's *RiscFree*[™] IDE and Debugger under Windows and Linux.



Opella-XD Highlights

- 3MB/s download speeds making it suitable for large, complex, software-intensive projects
- Fine-grained adjustment of JTAG clock frequency from 1kHz to 100MHz
- Auto-conditioning ensures maximum possible download speed with fastest JTAG clock frequencies
- Hot-plug support – allows connection to a running target without resetting or halting
- Opella-XD supports Multi-core debug for devices containing multiple RISC-V cores

Opella-XD Features

- Supports 32-bit and 64-bit RISC-V devices
- Powered by USB2 interface – no external power-supply required
- Fast, trouble-free "Plug-and-play" installation and configuration
- Opella detects and automatically configures for the appropriate target voltage
- Display/read/write of target system memory and peripheral registers
- Support for on-chip hardware breakpoints – unlimited software breakpoints
- Run/stop control of target application including go, halt, step over, step into and step out of
- Configurable Target-Reset and Test-Port-Reset, under full user control
- Built-in diagnostics instantly show status of Target, Debug Probe and USB link

FEATURES OVERVIEW	Opella-XD
Supported architectures	ARC, ARM, MIPS, RISC-V
Max JTAG speed	100MHz
Download speed	3MB/s
Target Voltage Range	0.9V - 3.6V
Extras	Auto-conditioning and Hot-plug

Order Codes

PRODUCT	Order Code
Opella-XD High Performance Hardware Debug Probe for RISC-V with Target Cable	Opella-XD-RISCV

Ashling USA - HQ
44901 Falcon Place
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