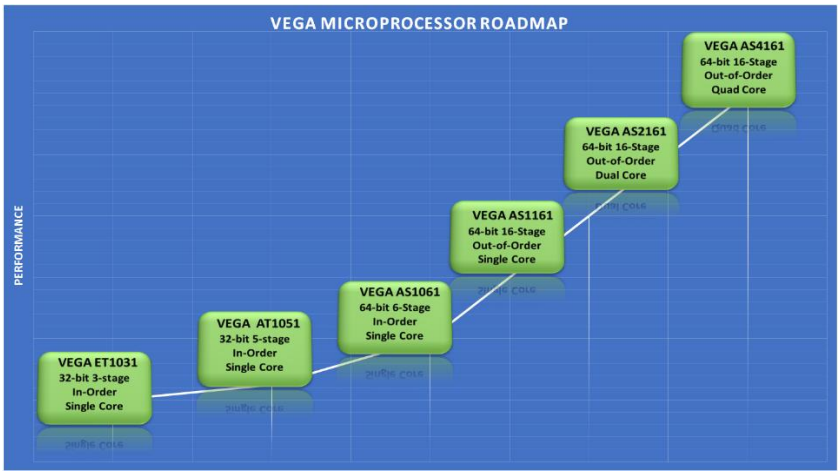
Ashling announces *RiscFree*™ C/C++ SDK support for India's C-DAC VEGA RISC-V-based Multi-core Microprocessors

July-8th, 2024, Kochi, India. Embedded tools developer Ashling is pleased to partner with C-DAC, supporting their **VEGA** RISC-V based multi-core microprocessor family with our ***RiscFree***™ C/C++ SDK and ***Opella-XD*** Debug Probe.

"Professional toolsets and a broad ecosystem are critical for the commercial growth and swift advancement of RISC-V technologies, and we are excited to work with an industry leader like Ashling to augment our capabilities for customers and provide strong support for our VEGA RISC-V multi-core microprocessors through a complete toolchain." **– Krishnakumar Rao, Senior Director and Head, Hardware Design Group, C-DAC Trivandrum, India.**

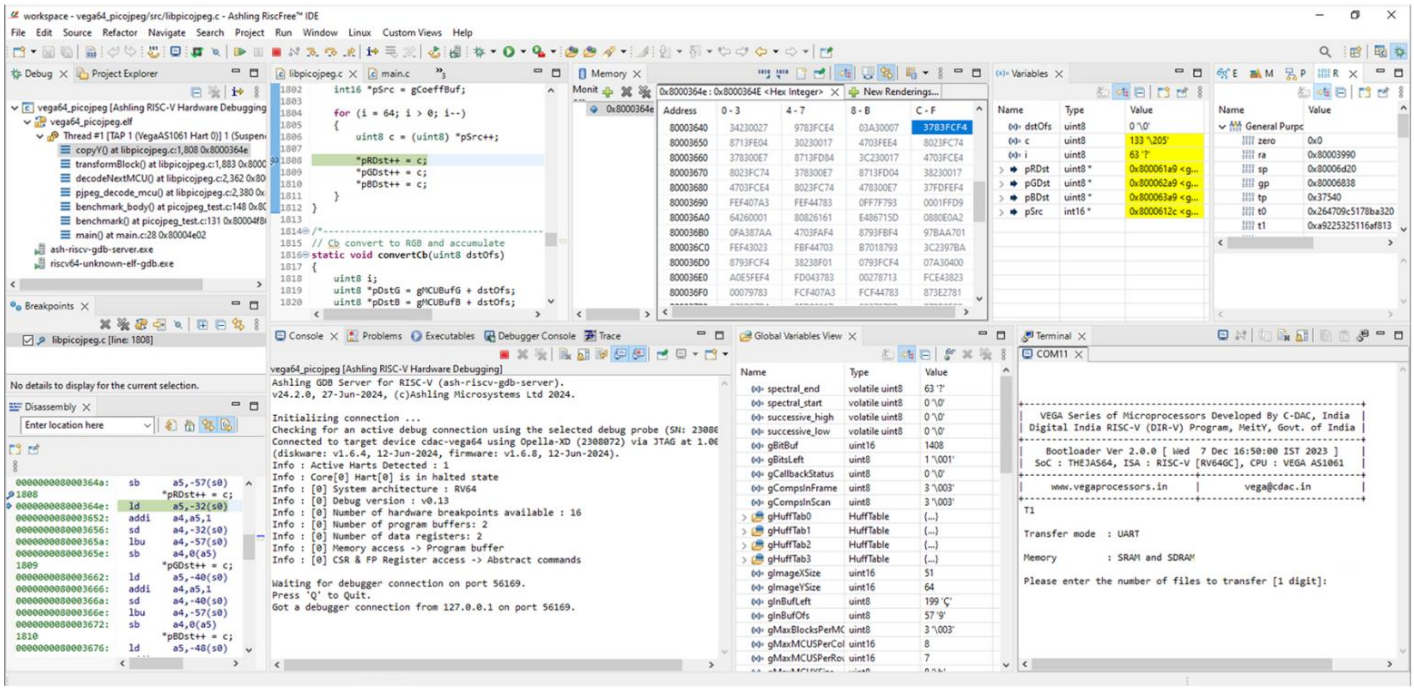


C-DAC VEGA Microprocessor Roadmap

RiscFree is Ashling's SDK including an IDE, compiler and debugger and provides software development, debug & trace support for RISC-V cores. Since its introduction, Ashling's ***RiscFree*** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development. Ashling has a particular focus on RISC-V and is the first to bring tools to the market supporting heterogeneous, simultaneous, multi-core debugging and tracing of both RISC-V and Arm cores.

*"Since launching, Ashling's **RiscFree** SDK has rapidly gained momentum in the embedded tools landscape, particularly in the RISC-V arena, and is praised for its user-friendly design, comprehensive features, modular structure, and solid support for both multi-core and real-time trace functionality. Our partnership with C-DAC allows their end-users to leverage the exceptional performance of the VEGA multi-core, RISC-V microprocessors, further enriching our suite of products and establishing a new benchmark in software development tools for both 32-bit and 64-bit RISC-V environments."* **– Ravi Nuguri, Strategy and Business Development Advisor, Ashling India.**

RiscFree C/C++ SDK



Ashling's RiscFree SDK Debug View

Ashling ***RiscFree*** SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multi-core debug support.
- ***RiscFree*** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Automatic source-code formatting, syntax colouring & function folding.
- Integrated compiler toolchain.
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators.
- High-level RISC-V register viewer.
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples.

For more information or to download a free evaluation of Ashling's ***RiscFree*** see: https://www.ashling.com/ashling-riscv/ and for details on the C-DAC VEGA RISC-V microprocessors visit here: https://vegaprocessors.in/

About Ashling

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting heterogeneous, multi-core debugging of RISC-V cores along with other cores from other vendors, for example, Arm-Cortex. Visit https://www.ashling.com/ for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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