Ashling and InCore announce Ashling’s *RiscFree™* C/C++ SDK support for InCore’s RISC-V-based Azurite Cores.

October 17, 2023, Chennai, India and Limerick, Ireland. Fabless processor core IP provider InCore Semiconductors and embedded tools developer Ashling today announced support for the Azurite family of RISC-V processor cores from InCore in Ashling’s *RiscFree* software development kit (SDK) and *Opella-XD* Debug Probe.

*RiscFree* is Ashling’s SDK including an IDE, compiler and debugger and provides software development, debug & trace support for the RISC-V. Since its introduction, Ashling’s *RiscFree* SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to choice for 32-bit and 64-bit RISC core software development.

InCore’s Azurite family of cores is an extremely efficient implementation of the RISC-V ISA, optimised for very low area and power. The Azurite family supports multiple RISC-V ISA extensions like PSIMD, bit manipulation, floating point and integer-multiply-divide. Azurite can be used in traditional 8-bit and 32-bit applications such as sensor fusion, wearables, motor control, smart IoT and analog mixed signal processing.

“Ashling has been a great partner with their comprehensive toolchain that empowers developers in their adoption of RISC-V. Enabling Ashling’s IDE and debug probes on our processors helps our customers develop solutions and get to market faster with InCore’s RISC-V offerings.” - Niraj Sharma, Chief Product Officer at InCore.

"We’re delighted to now include support for InCore’s Azurite RISC-V core and both our engineering teams are lined up for further collaboration ensuring upcoming Azurite core debug and trace features are supported as they become available." - Hugh O’Keeffe, CEO of Ashling.
Ashling **RiscFree** SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multi-core debug support
- **RiscFree** includes a single-shot installer that installs & automatically configures all the component tools to work “out-of-the-box”
- Automatic source-code formatting, syntax colouring & function folding
- Integrated compiler toolchain
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators
- High-level RISC-V register viewer
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples

For more information on Ashling’s **RiscFree** see: [https://www.ashling.com/ashling-riscv/](https://www.ashling.com/ashling-riscv/) and for details on InCore’s Azurite RISC-V core: [https://incoresemi.com/core-gen.html](https://incoresemi.com/core-gen.html)

**About Ashling:**
Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit [www.ashling.com](http://www.ashling.com) for more details.

**About InCore:**
InCore Semiconductors is a fabless core IP & chip design startup building fully customizable RISC-V cores and reference SoCs, to create high-performance, low-power, and cost-effective solutions for a variety of embedded applications. The founding team at InCore was previously responsible for the creation of Shakti - India’s first indigenously designed microprocessor, at the RISE lab at IIT Madras. Visit [https://incoresemi.com](https://incoresemi.com) for more details.

**About RISC-V**
The RISC-V open architecture ISA is under the governance of RISC-V International. Visit [https://riscv.org](https://riscv.org) for more details.

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