



Ashling announce *RiscFree*[™] support for MachineWare's SIM-V RISC-V Instruction Set Simulator.

Limerick, Ireland. 29th May 2023.

Ashling announced today that Ashling's *RiscFree* SDK now provides target debug support for MachineWare's **SIM-V** RISC-V Instruction Set Simulator.

RiscFree is Ashling's SDK including an IDE, compiler, libraries and debugger and provides software development and debug support for RISC-V. Since its introduction, Ashling's *RiscFree* SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace have made it the go-to choice for 32-bit and 64-bit RISC-V software development.

	SIM-V - SIM-V_Sample/src/main.c - Ashling Ris	icFree™ IDE	
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▼ SIM-V_Sample [GDB Hardware Debugging]	136 return 0; 137 }	Enter location	here 🐑 👔
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	1390/************************************	150	char szSl
main() at main.c:160 0x80000358	141 * Engineer: Sandeep V L	80000336: 23 2c 04 fc 8000033a: 23 2e 04 fc	
/home/testuser/Ashling/riscv32-unknown-elf/bin/riscv32-unknow	n 142 * Input: None	8000033e: 23 20 04 fe	
2003aA 92 2007 1296 06 2017	143 * Output: Always 0 144 * Description: Main function of demo.	80000342: 23 22 04 fe	sw zer
	145 * Date Initials Description	80000346: 23 24 04 fe	
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GRP(General Registers).REG(pc) Unsigned / F 0x80000358	<pre>152 /* Initialize SPI Configuration Register */ 153 SPI CR.uiRegValue = 0;</pre>	80000358: 17 05 00 00	
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	155 /* Configure SPI module */	161	ReadS
	156 ConfigSPI(); 157	80000362: 93 07 84 fd	
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Type Value	<pre>#160 WriteSPI("Hello! I am SPI Master."); 161 ReadSPI(szSlaveMessage);</pre>	8000036a: 93 07 84 fd	addi a5,
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char [24] 0x80000f80	163 }	80000370: 81 45 80000372: 3e 85	li al, mv a0,
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	Find the GDB manual and other documentation resources online at: http://www.gnu.org/software/gdb/documentation/ >.		
🗹 🖉 [address: 0x80000360]	<pre><nctp. documentation="" gub="" sortware="" www.gnu.org=""></nctp.>.</pre>		
🛛 🖉 main.c [line: 160]	For help, type "help".		
🛃 👦 main.c [line: 162] [type: Hardware]	Type "apropos word" to search for commands related to "word". (gdb) startup () at/src/startup.S:10		
	10 la gp, global pointer\$		
	Temporary breaknoint 4 main () at /crc/main c·150		

Figure 1. RiscFree connected to MachineWare SIM-V

"We are excited to offer our customers target debug support for the MachineWare SIM-V simulator" said **Hugh O'Keeffe, CEO of Ashling**. "This collaboration between Ashling and MachineWare enables developers to accelerate their RISC-V software development, testing, and debugging, ultimately leading to faster time-to-market for RISC-V-based products."

MachineWare's **SIM-V** is a RISC-V simulator that enables developers to test and verify RISC-V based systems and software applications. The simulator provides a high-performance Instruction Set Simulator (ISS) that supports all RISC-V standard extensions, including privileged ISA and custom instructions. The intuitive **SIM-V** extension allows quick addition of custom instructions and registers to **SIM-V** to get immediate feedback on design choices.

⊡	testuser@testuser-ThinkCentre-M90s: ~/Downloads/sim-V/simv-vp-v2023.04.20/bin		
testuse	r@testuser-ThinkCentre-M90s:~/Downloads/sim-V/simv-vp-v2023.04.20/bin\$./simv-vp -f /home/testuser/Downloads/sim-V/simv-vp-v2023.04.20/sw/rv32/dhrystone-2.2-x1.cfg		
SystemC 2.3.3-MachineWare GmbH Apr 20 2023 19:10:42 Copyright (c) 1996-2018 by all Contributors, ALL RIGHTS RESERVED			
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Figure2. Invoking MachineWare SIM-V.

"MachineWare is excited to work with Ashling to bring this solution to the RISC-V community" said Lukas Jünger, Managing Director with MachineWare. "The combination of Ashling's RiscFree SDK and MachineWare's SIM-V simulator provides developers with a powerful and flexible solution for simulation-based RISC-V software development, enabling them to develop high-quality applications more efficiently and begin target debug before hardware availability."

Ashling's **RiscFree** SDK with support for the **SIM-V** simulator is now available and for more information, please visit the Ashling website at <u>https://www.ashling.com/ashling-riscv/</u> for more on our RISC-V tools.

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East and America. Visit <u>www.ashling.com</u> for more general details.

About MachineWare

Founded in 2022 in Aachen, Germany, MachineWare leverages decades of experience in system level simulation and high-performance simulation tooling. Visit <u>https://www.machineware.de/</u> for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit <u>https://riscv.org</u> for more details.

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