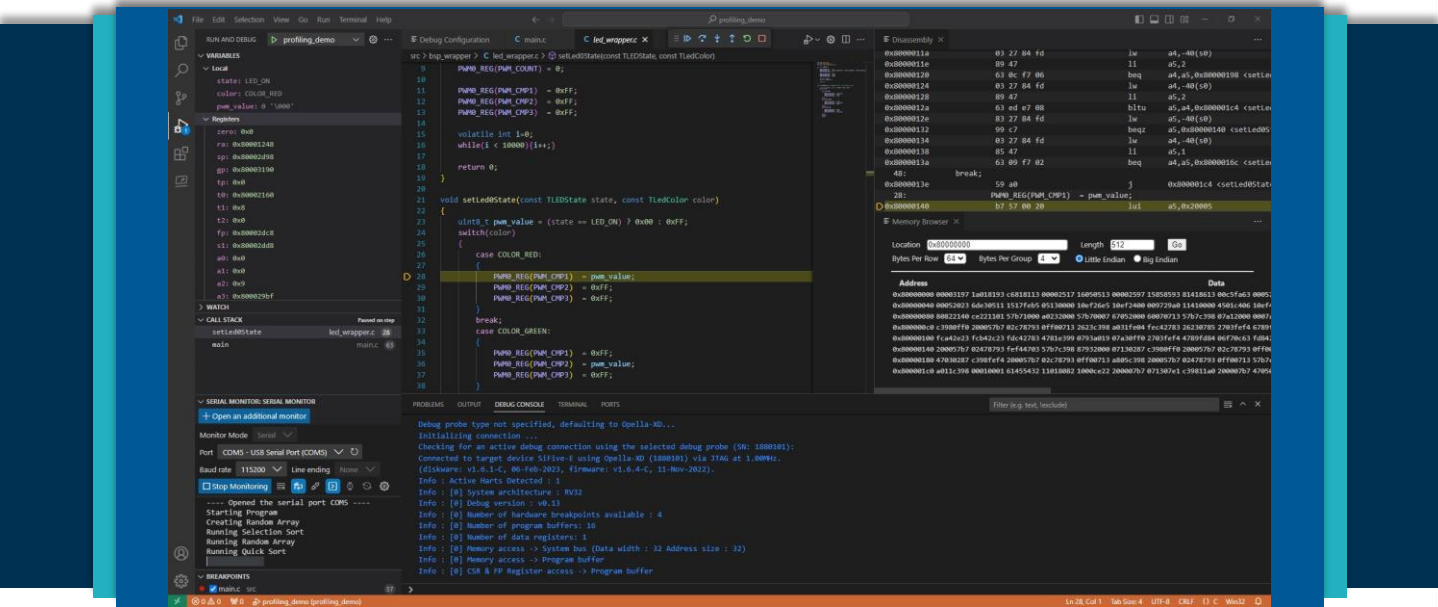


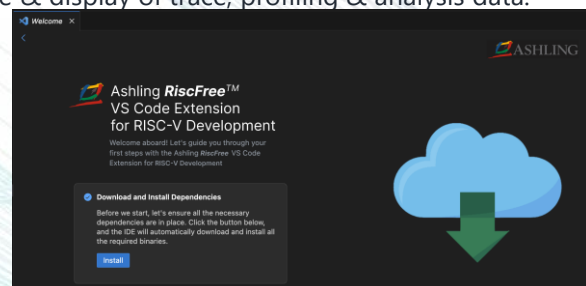
RiscFree™

Visual Studio Code Extension for RISC-V Development



Features

- Fully integrated into **Visual Studio Code (VSC)** with source-code & project creation, editing, build & debug support all for RISC-V development.
- Works with Windows and Linux Hosts.
- Includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Integrated GCC and/or LLVM RISC-V compiler toolchains.
- Project wizards, templates and examples.
- GUI based target debug configuration (no more *launch.json* file edits!)
- Ashling **Opella-XD** and **Vitra-XS** hardware debug & trace probes support fully integrated into the **VSC** debugger allowing hardware-based debug & easy setup, capture & display of trace, profiling & analysis data.
- Heterogeneous (e.g., Arm-Cortex + RISC-V) & homogeneous debug & trace support for multi-core SoCs sharing a single debug and/or trace interface is provided.
- On-chip and off-chip trace/debug analytics support.
- ROM or RAM based debugging support (e.g., hardware breakpoints for flash-based support).
- Integrated QEMU ISA simulator for 32-bit & 64-bit cores.
- Support for other industry standard instruction & cycle accurate simulators.
- High-level register viewer.
- Integrated RTOS (e.g., FreeRTOS or Zephyr) & OS (e.g. Linux) debug support.
- Fully scriptable debug interface using Python or GDB syntax.
- Support for SoC wide breakpoints i.e., a single breakpoint can halt all cores in active debug launches.
- Core dump debugging allows post-crash debugging and analysis using a core dump file.
- Supports core-specific software breakpoints in shared code i.e., only halt a specified core is running for common code shared between multiple cores.
- Support for advanced features including Docker Containers, AI-powered coding features found in GitHub Copilot and secure, cloud-based development environments provided by GitHub Codespaces.



Product

RiscFree Visual Studio Code Extension for RISC-V Development

Order Code

RF-VSCEXT-RV

